Abstract

This thesis describes the development of an enhanced fabrication scheme for superconductor-insulator-superconductor (SIS) junction devices and its implementation into regular fabrication at the KOSMA microstructure laboratory. The SIS junctions discussed in this thesis are used as frequency mixers in radio astronomical heterodyne receivers and provide quantum-limited performance and best possible sensitivity in the millimeter and submillimeter wavelength region. SIS mixers consequently are standard instrumentation for spectroscopic measurements between 80 GHz and 900 GHz. New generation SIS mixers demand more accurate fabrication of the devices than is possible with exclusively UV photolithographic based processes. Two examples for such new generation SIS mixer devices are the 640–800 GHz KOSMA Band 2 mixer contribution to the HIFI instrument of the Herschel Space Observatory and mixers for the SMART multi-pixel, dual frequency (475 GHz and 810 GHz band) receiver installed at the Gornergrat observatory in Switzerland. Requirements to device fabrication are further aggravated with future projects, which will extend SIS mixer application above 1 THz.

The influence of fabrication tolerances on simulated device RF performance, in particular submicron junction area reproducibility and the alignment accuracy of the integrated tuning circuit top electrode with respect to the junction position, will be discussed with help of the design of the SMART 475 GHz devices. As a result device design demands a junction area reproducibility of $\pm 5\%$ for $0.6\,\mu\mathrm{m}^2$ areas in order to meet the requirements for sensitivity and input bandwidth. In addition, the integrated tuning circuit top electrode alignment accuracy must be better than $0.3\,\mu\mathrm{m}$ in order to comply with RF band center position requirements.

In comparison, photolithographic definition typically yields relative junction area reproducibilities $\Delta A_J/A_J$ worse than $\pm 20\%$ for $0.6\,\mu\mathrm{m}^2 < A_J < 1\,\mu\mathrm{m}^2$ and alignment accuracies not better than $\pm 0.7\,\mu\mathrm{m}$. Device yield for even smaller junction areas, e. g. as required for THz frequency mixers, is negligible. Consequently, two new processes with more accurate electron beam lithography (e-beam) based definition of the junction area as well as the integrated tuning circuit top electrode features have been developed with this thesis.

During fabrication of a SIS device a process is needed to remove the junction insulation material from the junction's top electrode in order to enable contacting to the top electrode of the integrated tuning circuit. Whereas the UV photolithography scheme uses a self-aligned niobium etch process (SNEP), which employs a photoresist stencil lift-off of the insulation layer, this can not be carried out with the thin e-beam resist layer. Therefore a chemical mechanical polishing (CMP) process for planarization of the SiO_2 junction insulation and integrated tuning circuit dielectric layer was developed. CMP is terminated upon clearance of the junction top electrode and thus replaces the lift-off process. This PARTS (planarized all-refractory technology for low T_c superconductivity) scheme was invented by IBM in the eighties and has the advantage of yielding a planar junction top electrode and dielectric interface.

CMP process development started from scratch and within the scope of this thesis could be developed to a mature process used in regular fabrication, e. g. for the HIFI Band 2 devices that have to undergo a rigorous space-qualification process. SiO_2 layer planarity results of ± 20 nm are readily achieved across the 20 mm diameter device area of the fused quartz wafer, which is sufficient for reproducible device performance and ensures high fabrication yield. Surprisingly, CMP yields a very clean junction top electrode surface, which enables a very good contact of the junction to the integrated tuning circuit top electrode. This has very beneficial influence on the device's DC I-V characteristics and device yield. Results presented with fabricated HIFI Band 2 devices clearly show that device gap voltage of these embedded trilayer type devices is systematically 0.2 mV higher and less scattered. Up to 90% device yield is achieved for the HIFI devices, which is a 60% improvement over the photolithographic fabrication scheme.

Development of the e-beam definition processes profited from the existing e-beam lithography system developed for hot-electron bolometer device definition. PMMA resist is used during definition of the junction areas and the pattern is transferred into the SIS trilayer either with a SiO_2 or an aluminum etch mask and subsequent reactive-ion etching (RIE). Junction area reproducibility for the HIFI devices has clearly improved but presently is still limited by the RIE process. These devices require a three-step RIE through all three junction layers and consequently demand a higher etch anisotropy for the process. On the other hand, devices which only require a one-layer RIE show a significantly improved relative junction area reproducibility of $\Delta A_J/A_J \leq 5\%$ for areas down to $0.6\,\mu\mathrm{m}^2$. This lies within specs for the SMART 475 GHz devices. SIS junctions with deeply submicron areas down to $0.1\,\mu\mathrm{m}^2$ were fabricated with excellent subgap leakage currents which confirms further development potential of the e-beam / CMP scheme.

E-beam definition of the top electrode of the integrated tuning circuit uses AZ5206 photoresist. The superior overlay accuracy of the e-beam system is demonstrated to be better than 200 nm. No influence of the e-beam writing on the junction's barrier characteristic is observed in the DC I-V curves. Unfortunately, mixer noise temperatures of these devices are much higher than expected. Analysis of the RF measurements indicates a contamination problem of the integrated tuning circuit top electrode niobium layer in case e-beam definition is employed. Devices fabricated with conventional photolithographic tuning circuit top electrode and e-beam junction area definition, however, show similar performance as SNEP processed devices. It is assumed that the contamination problem is photoresist-related and thus solvable.

Integration of the e-beam / CMP process for junction definition has been successfully demonstrated with the measured RF performance of HIFI Band 2 devices for frequencies between 640 GHz and 800 GHz. Mixer noise temperatures as low as $T_m = 53$ K (DSB) are achieved around 700 GHz (corresponding to less than $2h\nu/k$) and T_m stays below 200 K across the specified RF bandwidth of 160 GHz (corresponding to 22% relative input bandwidth). Mixer performance thus lies within reach of the baseline requirements for the HIFI instrument.

In summary, the e-beam / CMP based fabrication scheme is qualified for new generation device requirements and exhibits enough development potential for future THz frequency SIS mixer designs. In contrast to former photolithographic junction area definition, reproducibility of the junction area is now only limited by the RIE process. In particular, CMP must be judged as a very promising approach for submicron area SIS mixer device fabrication.